Hardware-in-the-loop Implementation of a Hybrid Circuit Breaker Controller for MMC-based HVDC Systems

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***Abstract*—This paper presents a hardware-in-the-loop (HiL) implementation of hybrid circuit breaker (HCB) controllers for the half-bridge modular multilevel converter (HB-MMC) based high-voltage direct current (HVDC) system protection. The HCB controllers with auto-reclosing and fault current limitation capabilities are implemented in a digital signal processing (DSP) board and tested by interfacing it with a HB-MMC based point-to-point (PTP) - HVDC system based on a real-time digital simulation (RTDS) platform. Detailed results for the operation of HCBs based on the RTDS are presented. The results demonstrate the performance of HCB controllers implemented in DSPs during DC-faults including the auto-reclosing operation and fault-current limiting capability.**

***Index Terms*—Digital signal processing board, Hardware-in-the-loop, real-time digital simulation, high-voltage direct current, hybrid circuit breaker controller**

I. Introduction

Half-bridge modular multilevel converter (HB-MMC) is the state-of-the-art topology for voltage-source converter (VSC) based high-voltage direct current (HVDC) systems owing to its flexibility, scalability to high voltage ratings, and wide power handling ability with lower voltage rated power semiconductors and DC capacitors [1], [2]. However, HB-MMCs suffer from DC-fault blocking limitations: when the MMC sub-modules (SMs) are blocked for protection, the shunt freewheeling diode acts as an uncontrollable rectifier with the AC-grid feeds the DC fault [3], [4]. Presently, DC fault protection solutions include the use of: *i)* fault tolerant converters (FTCs), *ii)* AC side circuit breakers (CBs) or *iii)* DC CBs [5]. However, the first two options have limitations: the cost and power losses of FTCs are high and AC side circuit breaker operations are too slow for DC-fault protection [6], [7].

Circuit breakers are required to isolate faults without damaging any circuit component and to conduct high current with low losses [8]. However, classical HVDC CBs do not meet these requirements. Presently, the most promising solution is the hybrid circuit breaker (HCB) [8].

Real-time digital simulation (RTS) is a common approach for power system simulation and testing with high accuracy and safety [8], [9], [10]. RTS (Fig. 1) offers the capability to interface hardware with simulations (Hardware-in-the-loop or HiL simulation) and the performance of the HCB controller can be tested without connecting it to the real HVDC system. Through RTS the transient and dynamic responses of HB-MMCs can be derived so that the real-time HB-MMC based HVDC simulation enables the validation of a hardware HCB controller via HiL.

Fig. 1. Real-time digital simulator at UNSW Sydney.

This paper discusses the HB-MMC based HVDC fault characteristics and existing protection technologies, develops the HCB controller in a DSP board with the capability of protecting an HB-MMC based HVDC system during transient and permanent pole-to-pole DC-faults and tests the controller by interfacing it with a benchmark HB-MMC based HVDC system implemented in an RTDS. The major contribution is the development and testing of HCB controller in a DSP board for use with RTS models, eliminating the need for software implementation and reducing the RTS computational requirements for a HB-MMC based PTP-HVDC system. The controller integrates fault current limitation (FCL) and auto-reclosing functions with the over-current fault detection method.

The paper is organized as follows. Section II analyses the HB-MMC based HVDC DC-fault and Section III reviews DC-fault protection technologies. Section IV describes the HCB model and Section V briefly discusses the fault detection and protection scheme. Section VI discusses HCB controller development. The operation and performance of the HCB controller is presented in Section VII. Finally, the conclusions are summarized in Section VIII.

II. HB-MMC Based HVDC DC-fault Analysis

Typically in power systems, faults are temporary, caused by lightning strikes, accidental contact with adjacent objects, extreme weather conditions etc. A DC fault on an HVDC

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system can be divided into two categories: pole-to-pole fault and pole-to-ground fault.

Pole-to-pole fault is a result of the two poles of the HVDC system coming in contact. Although it is a rather rare occurrence, it is regarded as the worst case fault in HB-MMC based HVDC systems. Regardless of the DC pole-to-pole fault location, the fault current would go through three stages [11].

The first stage is the *capacitor discharge stage*, which begins when the DC fault occurs and continues until the MMCs are blocked. During this stage, not only the AC-grid feeds the fault through the lower diode of each MMC SM as a three phase AC fault [12], but also SM capacitors start discharging through the upper IGBTs of the SMs. Therefore, the fault current is the superposition of two currents, and the SM capacitors discharging current is the dominant component [12].

The second stage is called *diode freewheeling stage*, which begins when the IGBTs of HB-MMCs are blocked. During this stage, IGBTs are opened and capacitors stop discharging, and all the fault current is commutated into to the lower diode of SMs. All six MMC arms act as diode stacks, where each arm carries a third of the cable current [13]. The last stage is the *grid-side current feeding stage* where the AC grid contributes to the DC fault in this stage. The three MMC arms act as an uncontrollable three-phase rectifier [11].

Higher inductance limits the fault current rising rate, while higher value of resistance reduce the peak current [14]. Thus, the shorter the distance between fault location and MMC HVDC converter stations, the faster the fault current rising rate and the higher peak current value. Pole-to-ground faults are more common but less harmful to the system when compared with pole-to-pole faults, which occur when the cable conductor touches the ground directly. The diode frewheeling stage is eliminated in, while the other two stages of pole-to-pole faults are present in pole-to-ground fault [15], [16].

III. DC Fault Protection Technologies for HB-MMC Based HVDC

Due to the DC fault blocking limitation of the HB-MMC, additional protection technologies are needed to isolate a DC fault. Presently, there are three protection technologies for VSC-HVDC systems, which are analysed in the following sections.

A. AC side breakers

AC CBs are placed between the MMCs terminals and the AC grid. To interrupt a fault for AC system, the arc always happens in AC CBs. AC CBs could open without any arc at zero current. Typical AC CBs, including oil, air, gas and vacuum CBs, are able to interrupt the current in 3 to 5 cycles after receiving a trip signal from the protection relay which is about 2 cycles [7]. However, the fault current rises faster in HVDC because the impedance of HVDC transmission cables is lower than HVAC's. Therefore, slow AC CBs can not protect the HB-MMC based HVDC systems effectively.

B. Fault tolerant converters (FTCs)

FTCs use modified MMC SM designs to achieve DC fault isolation functionalities. There are two different categories of SMs: unipolar SMs and bipolar SMs [6]. Unipolar SMs only provide positive or zero voltage levels with simple topologies but lack DC fault blocking capabilities. Bipolar SMs, which are also called as fault tolerant converter (FTC) cells, can zero the DC side voltage of the MMC for DC fault isolation by reversing the SM voltage. However, typical bipolar SMs require increased numbers of power semiconductor devices to block DC-fault, leading to higher power losses and cost [6]. As a compromise between cost, efficiency and fault tolerance, hybrid structures combining unipolar and bipolar SMs have been proposed (see [17] for example).

C. DC breakers

DC CBs can be divided into three categories: mechanical, solid-state and hybrid [8].

Mechanical circuit breakers (MCBs) use a mechanical switch as their main interruption component. MCBs have low conduction resistance, as low as 10 $\mu\Omega$ [18]. When a fault occurs, the mechanical contacts are separated and an electric arc forms between the contacts of the breaker. Unlike AC systems, there is no natural zero-current crossing during the DC fault to allow the arc to be extinguished and open the MCB without damaging it. Therefore, additional commutation circuits are essential to achieve zero-current crossing and eliminate the arc. There are two categories of DC MCBs: passive resonance MCBs and active resonance MCBs [19]. Passive resonance DC CBs create a zero current crossing with the self-oscillation of inductance and capacitance [19]. Active resonance DC CBs have faster operation speed, and its topology is similar to the passive resonance CBs except for the pre-charged capacitor and an additional switch [20]. The main disadvantage of the classic MCBs is that it takes a long time (up to 10 to 100 ms) to interrupt the DC fault.

Solid-state CBs (SSCBs) have a much faster interrupting speed compared to MCBs because SSCBs do not create arcs. However, as SSCBs use power electronics as the main component, their high conduction losses are the major issue. Besides, the cost of cooling system and the large number of the semiconductor devices also affect the feasibility of SSCBs for HVDC applications. SSCBs are typically designed with a parallel surge arrester or with a freewheeling diode [8].

IV. Hybrid Circuit Breaker

The hybrid circuit breaker was first proposed in [21]. It integrates solid-state switches with a mechanical breaker, an energy absorption branch and a residual DC current breaker. Fig. 2 depicts the structure of the HCB.

A. Hybrid Circuit Breaker Model

The primary branch contains a mechanical ultra-fast disconnector (UFD – S1) and a load commutation switch (LCS – T1). LCS consists of a few number of IGBTs with shunt diodes and

a pre-charged capacitor. This branch conducts current during normal operation to minimize losses [4].

The secondary branch consists of semiconductor switches as the main breaker (MB – T2) for their fast interruption capability. An additional parasitic inductor (L_p) is added to the secondary branch to obtain realistic commutation time [4]. The energy absorption branch is the key element of the circuit breaker, which contains a bank of surge arresters, aiming to limit the transient voltage and dissipate the excess magnetic energy from the grid [21].

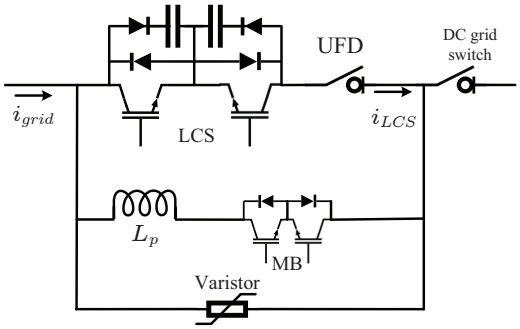

Fig. 2. Configuration of a hybrid circuit breaker.

B. Hybrid Circuit Breaker Controller

During normal operation, the LCS and UFD are turned on, current flows through the MCBs, resulting in low conduction losses. When the current reaches the potential fault threshold, the IGBTs of LCS open and the semiconductor switches of the secondary branch are turned on. The LCS's snubber pre-charged capacitor acts as a voltage source in the primary branch and assists in the commutation of the breaker current into the secondary branch of the HCB. Once the zero current crossing in the primary branch is detected, the mechanical UFD can be opened without arcs [4].

When the current flows through the secondary branch, the parasitic inductance reduces the current rise rate and the solid-state switches' turn on resistance limits the peak of the fault current. When the current rises to the fault confirmation threshold, MB could be opened to interrupt the fault current quickly. In the end, the surge arresters of the energy absorption branch can absorb the fault energy and the DC grid mechanical switch (S2) is opened to isolate the fault without arc [4].

To reclose the CB, the current first flows through the main breaker. If the current drops to zero, the UFD will be closed followed by LCS. The close function could be considered as a reverse operation of opening a HCB. Therefore, if a fault or potential fault is detected during the reclose operation, the HCB may open again.

V. Fault Detection and Protection Scheme

Over-current protection method is applied for fault detection [22]. When a pole-to-pole fault occurs, the fault current rises. To discriminate the fault, over-current protection needs to set a current threshold to confirm a fault. Before confirming a fault, there is an open grid (OG) threshold for the potential fault detection [4].

The additional functions of the HCB for the protection of a permanent or transient fault are discussed below:

A. Auto-reclosing operation

This function is similar to AC system protection. In AC system, auto-reclosing requires a dead time. When an AC-fault is detected, AC CBs open, delay and reclose a few times. For a long duration fault, HCB opens first, and delay for a short duration, then reclose to see whether the fault is cleared.

B. Fault current limitation

The HCB can control the fault current within a pre-set range without disconnecting completely [23]. In this scheme, the secondary branch and the energy absorption branch work as a solid state fault current limiter: when the main breaker is closed and the primary branch is opened, the fault current rises with a relatively slow rate; once the current reaches the upper bound of the pre-set range, the main breaker opens and the fault current decreases; then, the main breaker is turned on again when the fault current falls below the lower bound of the preset range [21].

Due to the lifetime limitation of the main breaker, HCBs cannot perform FCL infinitely. A reclose FCL operation will be repeated for a predetermined number of times, after that the HCB is opened permanently. The number of repeated operations for FCL is determined by the thermal tolerance and cooling system of the main breaker [4].

VI. Hybrid Circuit Breaker Controller Development

The HCB controller is implemented in a DSP board TMS320F28027 and interfaced with a HB-MMC based benchmark PTP-HVDC system. The HB-MMC models and controllers, HCB models, cable models and AC sources are simulated in one RTDS rack.

There are five user defined options implemented to interfacing of HCBs.

1) *DSP*: MMC blocking coordination signals and HCB switching signals are delivered from DSP board when DSP is 1.
2) *DCFAULT*: A DC pole-to-pole fault occurs when variable $DCFAULT$ is 1 and the fault is cleared after the preset duration.
3) *DCFLTduration*: This variable is used to control the duration for the DC pole-to-pole fault that is applied during the tests. The value of $DCFLTduration$ ranges from 0-100 s.
4) *FCL*: The HCBcontroller operates with FCL protection scheme when FCL is 1, and operates with auto-reclosing protection scheme when FCL is 0.
5) *ResetState*: The DSP controller resets when $ResetState$ is 1.

The interface between RTDS and DSP is shown in Fig. 3. RTDS delivers '$ResetState$' and 'FCL' signals as well as the

measurements of HCBs' primary branch and DC cable current to the DSP board via an analogue output (GTAO) card. These current measurements are scaled in RSCAD in order to make the RTDS outputs $3.3V$ maximum to match the voltage rating of DSP analogue digital conversion (ADC).

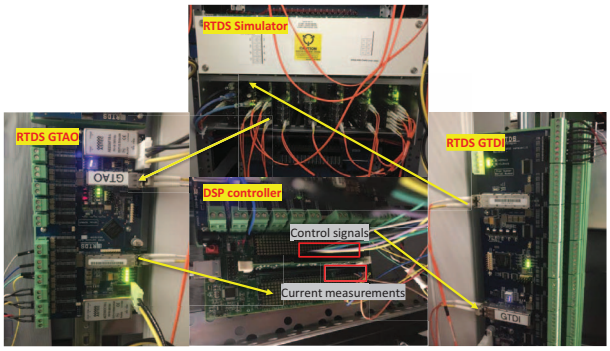

Fig. 3. Interface between the real-time simulator and the DSP.

There is a state flow program runs inside the DSP: at each time step, the next state is decided based on the present state and receiving analogue outputs from the RTDS GTAO. Afterwards, the DSP delivers digital signals to control the HCBs switches and MMCs via a digital input (GTDI) card.

There are four HCBs in the HB-MMC HVDC system, and each pair of HCBs are controlled by the same switching signals.

A. HCB Controller operation

Each HCB consists of four switch blocks: two MCBs (*S1* that corresponds to the UFD *S2* that corresponds to the DC grid switch) and two SSCBs (*T1* that corresponds to the LCS and *T2* that corresponds to the MB). MMCs blocking protection (*S0* is the MMCs blocking trigger) is integrated with the HCB controller and the operating state can be represented with binary states ('1' for 'on', '0' for 'off'). The command to the HCB corresponds to a combination of the states of the above, arranged in the sequence from MSB to LSB: {S0, S2, T2, S1, T1}.

For the DSP controller program, there are four internal control signals for each of the HCBs and two common external control signals that apply to all HCBs operated by the one DSP. The functions of these signals are the following:

1) *Open Grid (OG)*: OG is 1 when primary branch current reaches open grid current threshold ($I_{LCS} > I_{OG}$).
2) *Commutation Limit (CL)*: CL is 1 when primary branch current is lower than commutation limit ($I_{LCS} < I_{CL}$).
3) *Fault Confirm (FC)*: FC is 1 when the current reach fault confirmation threshold ($I_{GRID} > I_{FC}$).
4) *Commutation Limit 2 (CL2)*: $CL2$ is 1 when the current is lower than commutation limit ($I_{GRID} < I_{CL}$).
5) *Fault Current Limitation (FCL)*: If FCL is 1 when FCL is used otherwise an auto-reclosing scheme is used.
6) *Reset (RESET)*: Resets the HCB when $RESET$ is 1.

The state flow chart of the HCB, as implemented in the DSP based on previous software implementation is shown in Fig. 4.

Each terminal's HCBs controller operates with an independent state flow chart. The blocking state of the MMCs at the two terminals of the HVDC system is also coordinated with the HCB controller[1].

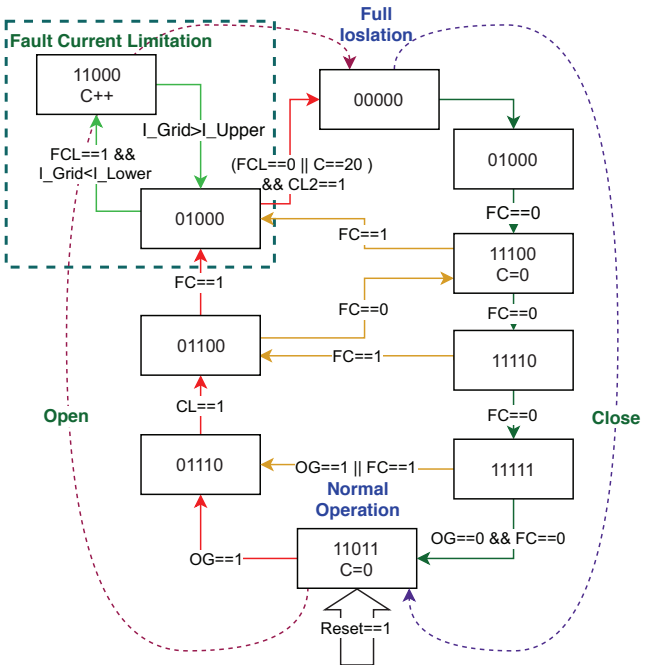

Fig. 4. HCB controller state flow chart (state bits arrangement: S0, S2, T2, S1, T1).

VII. Benchmark Case Study

As shown in Fig. 5, a 400MW HB-MMC HVDC system with a 183.5 km transmission cable based on the DC Test System 1 from CIGRE Working Group B4.57 is simulated in the RTDS [2], [9]. The rating of the HVDC system is shown in Table I, and Table II presents the HCBs component ratings. Steady-state results for the HVDC system are not provided due to space constraints, but they can be found in [2].

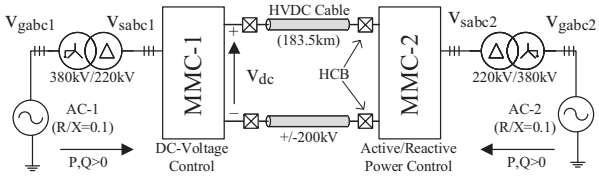

Fig. 5. Two-terminal HB-MMC based HVDC system.

A. Test of interrupting a pole-to-pole fault

In order to detect the DC-fault with the overcurrent scheme, the fault confirmation current threshold is set to 9 kA, the open grid current threshold for both controllers is set to 5

[1]A detailed explanation of the CB model implemented in the RTDS, the software implementation of the controller, HCB commands and an instruction manual have been made freely available for download at: http://tinyurl.com/UNSWUOM-UP . *Password*: DCCBPaper

TABLE I
MMC-HVDC SIMULATION PARAMETERS

Rated Power	400 MVA
Number of SMs/arm (N)	200
DC-Voltage (V_{dc})	400 ($\pm$200) kV
SM Capacitance (C)	10 mF
SM Capacitor Voltage (V_C)	2 kV
Arm Inductance (L)	29 mH
Transformer Leakage Inductance	35 mH
Transformer Resistance	0.363 Ω

TABLE II
HCBS COMPONENTS RATINGS

LCS RLC ramping factor	1.33 pu
UFD RLC ramping factor	1 pu
UFD extinguish arc for current at or below	0.05 kA
MB RLC ramping factor	1.33 pu
MB inductance	4 mH
Arrestor knee voltage	300 kV

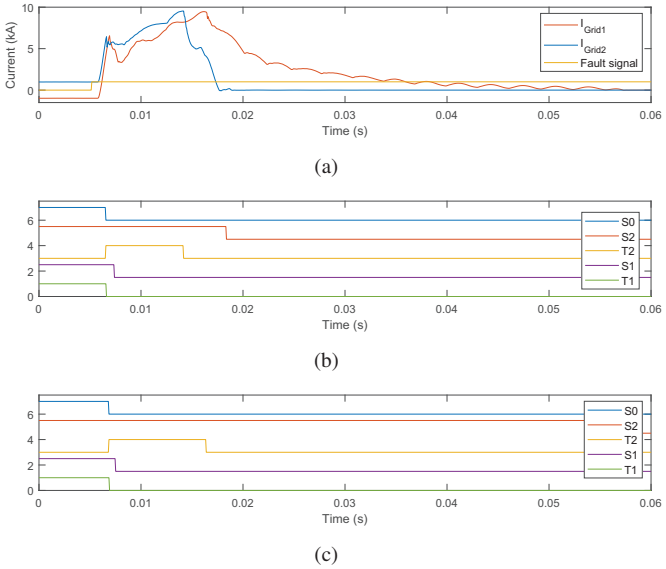

Fig. 6. Operation of HCB controllers, (a) Grid currents of the terminals, (b) HCB switching signals at T1, (c) HCB switching signals at T2.

kA, and the commutation current threshold is 0 kA [21]. Fig. 6 demonstrates the breaker operation performance and HCBs switching signals when a pole-to-pole fault occurs at the middle of the transmission cable.

The LCSs and MMCs at terminal 1 are turned off when fault current rises to 5.952 kA at t=6.8 ms with a 6.484 kA/ms rising rate and terminal 2 opens when the fault current rises to 5.698 kA at t=6.5 ms with a 6.247 kA/ms rising rate, while the fault signal is triggered on at t=5.18 ms. The peak primary branch currents for both cases are higher than the OG threshold. Because in this stage the fault current is contributed by both the AC grid and the discharging current of the HB-MMCs SMs capacitors, the fault current rise rate is faster than the DSP ADC response.

After switching off LCS and blocking MMCs, the primary branch current is commutated to the secondary branch rapidly. After the primary branch current drops to zero, the UFD at terminal 1 opens at t=7.46 ms and the UFD at terminal 2 opens at t=7.34 ms. Afterwards, the fault current flows through the secondary branch of the HCBs only. Due to the higher resistance of the MB and the additional parasitic inductance, the fault current has a lower peak and rising rate. When the HCBs secondary current reaches the fault confirmation limit, the MBs open instantly. After the energy absorption branch absorbs the resultant fault energy and the current drops to zero, the grid side MCBs may open without arcs.

The fault current at terminal 1 takes 9.5 ms to reach the FC threshold, and the fault current at terminal 2 takes 7.6 ms. The current rising rate at terminal 1 is 0.578 kA/ms and at terminal 2 it is 0.567 kA/ms. Thus, HCBs would only reclose after staying at state '01100' for 12 ms if the current does not reach the predefined threshold. Terminal 1 HCBs takes 11.2 ms to interrupt a 9.427 kA pole-to-pole fault, while the HCBs at terminal 2 take 8.9 ms to interrupt a 9.534 kA pole-to-pole fault.

B. Test of HCBs controller with auto-reclosing operation

The auto-reclosing function of the HCB is implemented to allow differentiations between transient and permanent faults and allow for faster recovery of the HVDC system after a transient fault. The HCB auto-reclosing function is shown in Fig. 7(a). In this case, a long duration fault is considered to test the operation of the HCBs, after three successive reclosing operation a 'Reset' signal is issued and the HCBs stay open. In Fig. 7(b), the shorter duration transient fault is considered. The fault is cleared during the auto-reclosing operation, at which point the HCBs reclose and the system returns to normal operation after t=0.6 s. The HCBs switching signals are generated by the DSP and sent to the real-time simulation are shown in Figs. 7(c) and Fig. 7(d) for Terminals 1 and 2, respectively.

C. Test of HCBs controller with FCL operation

The FCL protection scheme is also tested for the protection of a transient fault. During FCL operation, the fault current at terminal 1 is limited between 1 kA and 3 kA to achieve the 2 kA average current, which matches the HVDC system current carrying capabilities [9]. When the fault is cleared (at t = 0.05 s) and during the FCL operation, the HCBs reclose and the HVDC system returns to normal operation. The results of FCL operation are shown in Fig. 8.

VIII. CONCLUSION

A hardware-in-the-loop implementation of a controller for a hybrid circuit breaker (HCB) for HVDC protection based on a DSP board is presented in this paper. The implementation reduces the processing requirements of an RTDS system also eliminating software-based control for the HCB. Results from pole-to-pole faults on a benchmark point-to-point HVDC systems demonstrate the functions of the DSP HCB controller

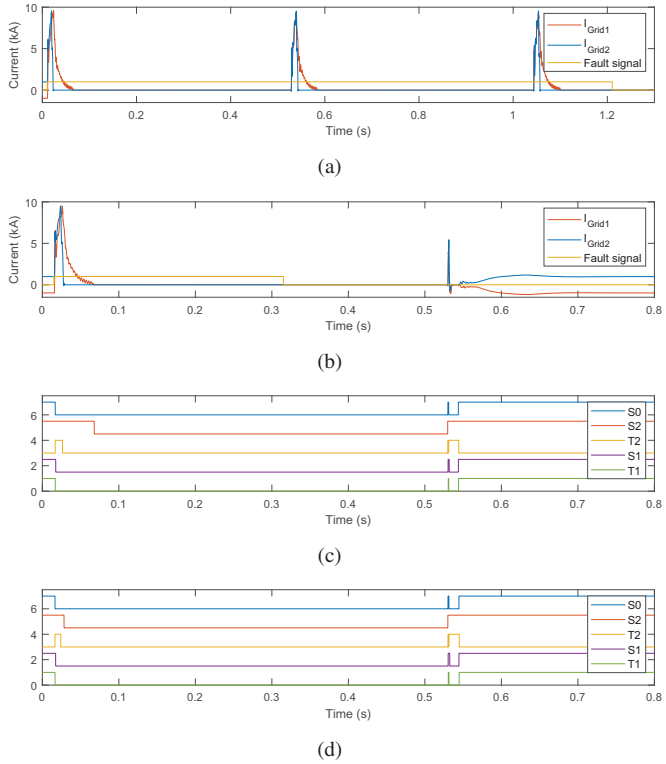

Fig. 7. HCB controller with auto-reclosing operation,(a) Long duration fault, (b) Short duration fault, (c)HCB switching signals at T1 with a short duration fault, (d) HCB switching signals at T2 with a short duration fault.

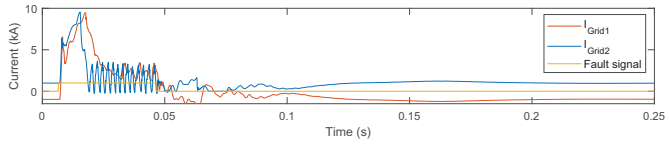

Fig. 8. Reclosing after FCL with a short duration fault.

in operating the HCB, including fault interruption, autoreclose and fault current limitation (FCL) functionalities. Based on the developed implementation it is possible to simulate a complete HVDC transmission system with HCBs using one RTDS rack instead of two with average MMC models and two racks instead of three with the switching MMC models.

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References

[1] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan 2015.

[2] H. R. Wickramasinghe, G. Konstantinou, J. Pou, and V. G. Agelidis, "Interactions between indirect DC-voltage estimation and circulating current controllers of MMC-based HVDC transmission systems," *IEEE Trans. Power Syst.*, vol. 33, no. 1, pp. 829–838, Jan 2018.

[3] E. Kontos, G. Tsolaridis, R. Teodorescu, and P. Bauer, "On DC fault dynamics of MMC-based HVDC connections," *IEEE Trans. Power Del.*, vol. 33, no. 1, pp. 497–507, Feb 2018.

[4] O. Cwikowski, H. R. Wickramasinghe, G. Konstantinou, J. Pou, M. Barnes, and R. Shuttleworth, "Modular multilevel converter DC fault protection," *IEEE Trans. Power Del.*, vol. 33, no. 1, pp. 291–300, Feb 2018.

[5] E. Spahic, F. Schettler, D. Varma, and J. Dorn, "Impact of the DC technology on transmission grids," in *Proc. IET ACDC-2015*, Feb. 2015, pp. 1–7.

[6] G. Konstantinou, J. Zhang, S. Ceballos, J. Pou, and V. G. Agelidis, "Comparison and evaluation of sub-module configurations in modular multilevel converters," in *Proc. IEEE PEDS-2015*, Jun. 2015, pp. 958–963.

[7] Y. W. Jeong, H. W. Lee, Y. g. Kim, and S. w. Lee, "High-speed AC circuit breaker and high-speed OCR," in *Proc. CIRED 2013*, Jun. 2013, pp. 1–4.

[8] CIGRE Joined Working Group A3/B4.34, "Technical requirements and specifications of state-of-the-art HVDC switching equipment," 2017.

[9] CIGRE Working Group B4.57, "Guide for the development of models for HVDC converters in a HVDC grid," 2014.

[10] H. R. Wickramasinghe, G. Konstantinou, Z. Li, and J. Pou, "Development of an alternate arm converter benchmark model for HVDC applications," in *Proc. IEEE IECON-2017*, Oct. 2017, pp. 4506–4511.

[11] J. Yang, J. E. Fletcher, and J. O'Reilly, "Short-circuit and ground fault analyses and location in VSC-based DC network cables," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3827–3837, Oct 2012.

[12] Z. Sun, F. Gao, Z. Li, Y. Luo, P. Wang, Y. Li, X. Yang, and R. Gou, "The analysis and experiment of DC-link short-circuit of modular multilevel converter based high voltage direct current system," in *Proc. IEEE ICIEA-2014*, June 2014, pp. 1287–1291.

[13] O. Cwikowski, A. Wood, A. Miller, M. Barnes, and R. Shuttleworth, "Operating DC circuit breakers with MMC," *IEEE Trans. Power Del.*, vol. 33, no. 1, pp. 260–270, Feb 2018.

[14] S. Ademi, D. Tzelepis, A. Dyko, S. Subramanian, and H. Ha, "Fault current characterisation in VSC-based HVDC systems," in *Proc. IEEE DPSP-2016*, March 2016, pp. 1–7.

[15] L. Lin, Z. He, J. Hu, Z. He, and K. Xu, "Pole-to-ground fault ride through strategy for half-/full-bridge hybrid MMC-based radial multi-terminal HVDC systems with low-impedance grounded," *IET Gener. Transm. Distrib.*, vol. 12, no. 4, pp. 1038–1044, 2018.

[16] M. K. Bucher and C. M. Franck, "Analytic approximation of fault current contribution from AC networks to MTDC networks during pole-to-ground faults," *IEEE Trans. Power Del.*, vol. 31, no. 1, pp. 20–27, Feb 2016.

[17] J. Qin, M. Saeedifard, A. Rockhill, and R. Zhou, "Hybrid design of modular multilevel converters for HVDC systems based on various submodule circuits," *IEEE Trans. Power Del.*, vol. 30, no. 1, pp. 385–394, Feb 2015.

[18] A. Greenwood, I. of Engineering, and Technology, *Vacuum switchgear*. Stevenage : Institution of Electrical Engineers, 1994.

[19] B. Pauli, G. Mauthe, E. Ruoss, G. Ecklin, J. Porter, and J. Vithayathil, "Development of a high current HVDC circuit breaker with fast fault clearing capability," *IEEE Trans. Power Del.*, vol. 3, no. 4, pp. 2072–2080, Oct 1988.

[20] M. B. T. Erikksson and S. Halen, "A low loss mechanical HVDC breaker for HVDC grid applications," *45th CIGRE Session, Paris*, pp. 1–8, Aug 2014.

[21] J. Häfner and B. Jacobson, "Proactive hybrid HVDC breakers – a key innovation for reliable HVDC grids," *Proc. CIGRE 2011 Bologna Symp., Bologna, Italy*, pp. 1–7, Sep 2012.

[22] M. N. Baran, M.E., "Overcurrent protection on voltage-sourceconverter-based multiterminal DC distribution systems," *IEEE Trans. Power Del.*, vol. 22, no. 1, pp. 565–574, 2007.

[23] K. Smedley and A. Abravomitz, *Development of fault current controller technology*. University of California, Irvine, 2011.