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Novel Piecewise Linear Formation of Droop Strategy for DC Microgrid

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***Abstract*—This paper proposes a new load current sharing control strategy for DC microgrid. It adopts the piecewise linear formation to adaptively assign droop gains to balance the load sharing accuracy with the deviation of bus voltage. Communication among the distributed units is unnecessary for the proposed operation. The approach is considered as a comprehensive solution to deal with the unbalanced performance in DC microgrid for different load levels. The balancing performance is shown by comparing with the traditional linear droop control and the latest nonlinear droop gain solution. The study is proceeded by the in-depth analysis of both steady state and system dynamics with simulation support. The claimed advantage is finally verified by both simulation and experimental evaluations.**

***Index Terms*—DC microgrid, piecewise linear, droop control, dynamics analysis.**

I. Introduction

DC microgrid (MG), which is the latest trend of electric systems, consisting of a local group of distributed energy resources (DERs) and energy storage systems (ESSs) [1]. The advance of power electronics enables DC voltage to be converted to different levels for various applications, such as high-voltage direct current (HVDC), telecommunication system, data centers, electronics factories, electric vehicles, renewable power generation, light-emitting diode (LED) lights and house applications [2]. Comparing to its counterpart of the AC MG, the DC system shows advantages of lower system cost, higher efficiency, and less concerns of transformer inrush currents, synchronization, skin-effect loss, and reactive power flow [3]–[5].

Due to the increase in distributed power generation and energy storage, an effective coordination strategy is important for DC MG to operate stably and robustly. Power converters are connected in parallel in DC MG and share the contribution from various sources to the loads, which requires a uniform power distribution scheme and effective coordination [6]. Otherwise, conflicts might happen and result in system instability. A complex DC MG includes significant numbers of converters, which can be remotely located. The infrastructure requires long cabling for interconnection, shows the difference in power capacity and demands for expandability [7]. The imbalance among converters may lead to the overloaded condition, and then cause system failure [8]. Alleviation of these issues requires an effective management scheme. The control of DC MG can be divided into three categories from the communication point of view [9]: (i) distributed control, (ii) centralized control (CC) and (iii) decentralized control.

Distributed control scheme is formulated that the central control unit does not exist and the local controllers communicate with each other via digital communication links (DCLs). It shows the advantage of robustness since it is less affected by the problem of the single point of failure. In particular, DC MG can retain full functionality even part of the DCLs fails since only the local information is transmitted via the DCLs [9]. When some units are not connected due to the DCLs failure, local controllers cannot access the information from other units. To prevent this problem and implement the level of awareness for local controllers like centralized control, the consensus algorithm is typically employed. The consensus algorithm is implemented within each local controller by summing up the differences of the variable(s) in a local controller and its neighbour [9].

Centralized control can be implemented by employing the indispensable CC and DCLs among all sources and loads in DC MG [9]. For a small scale DC MG, all local units via the high bandwidth DCL can be centrally controlled by using the master-slave approach. The master module controls the DC bus voltage, whereas the slave units control the current as commanded by the master module. For a large scale DC MG, the hierarchical control structure is often utilized since it defines the certain degree of independence between different control levels [10], [11]. The hierarchical control structure can be implemented by employing local converter control and system coordination control with DCLs. The hierarchical structure can be divided into three levels: the highest control level is to coordinate the overall DC MG for power management and protection function; the secondary control measures the MG voltage and adjusts the voltage reference for the primary controller; the primary controllers are implemented locally, which regulate individual converter's output voltage and balance the load sharing among all available sources [12]. Fast communication is generally required for high-performance coordination for both the master-slave operation and hierarchical control, which increases the cost and complexity. Such systems are generally vulnerable to communication failure [13].

Decentralized control is expected to be the most low-cost solution since it completely neglects communication link. However, the performance is generally limited due to the

Manuscript received Oct 09, 2018; revised Jan 15, 2019 and Mar 05, 2019; accepted Apr 07, 2019.).

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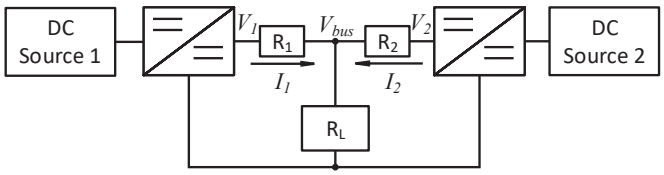

Fig. 1. DC MG system configuration

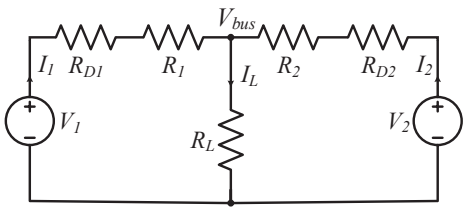

Fig. 2. DC MG equivalent circuit

lack of coordination among the distributed units [9]. Among all technologies, the droop method is widely applied, which decentralizes the control operation and performs load sharing and voltage regulation among distributed converters. The equalization of current sharing can be achieved by imposing a virtual resistance (VR) in each power conversion unit. Since the traditional droop implementation is based on a constant VR, its disadvantage lies in either poor voltage regulation or inaccurate current sharing [14], [15]. Nonlinear droop control is proposed by [16] to improve both voltage regulation and load sharing accuracy. The solution improves the performance of heavy load condition, however, it shows an unbalanced performance under the light load condition. One study proposed the piecewise linear droop control strategy, whose characteristic droop curve approaches to nonlinear characteristic droop curve as the numbers of segments increasing [17].

Other technologies can be optimally tuned and added to the droop scheme to achieve better performance, such as voltage restoration, adoptive droop control, model predictive control (MPC), and line resistance estimation. Communication links with low bandwidth of can be employed to minimize the DC bus voltage deviations [18], [19] and [20]. Adaptive droop gain can be achieved by using DCL in [21], [22]. The MPC can be integrated with the droop control for better coordination, as proposed in [23]. The line resistance measurement is proposed in [24] to adjust the droop gains by injecting the small-scale pulse perturbation voltage into the converter reference voltage and detecting the change of converter output.

Based on the existing development, this paper focuses on a novel piecewise linear formation of droop control scheme to improve the performance of load sharing accuracy and voltage regulation. During the system operation, the droop gain and nominal voltage level are adaptively adjusted according to the load condition without the requirement of the communication link. The paper is organized as follows. Section II analyses different DC MG control strategies. The proposed piecewise droop control strategy is elaborated in Section III. Small signal stability analysis is presented in Section IV. Section V shows simulation and experimental evaluations. The performance improvement is compared with other droop control approaches.

II. Review of Droop Operation for DC Microgrid

As an introduction, a simple DC MG configuration is represented in Fig. 1 showing two DERs and one common load. Its equivalent circuit is depicted in Fig. 2, where V_1, V_2 are the output voltages of converter 1 and 2, R_{D1}, R_{D2} represent the virtual droop resistance, R_1, R_2 symbolize the cable resistance, meanwhile, R_L is the load resistance.

Based on the equivalent circuit in Fig. 2, the bus voltage can be derived in (1) when the virtual droop resistances are assumed to be zero.

$$V_{bus} = \frac{R_L R_2 V_1 + R_L R_1 V_2}{R_L R_1 + R_L R_2 + R_1 R_2} \tag{1}$$

The shared current difference between the two converters becomes:

$$\begin{aligned}\Delta I &= I_1 - I_2 \\ &= \frac{R_L(V_1 - V_2) + V_1 R_2}{R_L R_1 + R_L R_2 + R_1 R_2} - \frac{R_L(V_2 - V_1) + V_2 R_1}{R_L R_1 + R_L R_2 + R_1 R_2} \\ &= \frac{2(V_1 - V_2)}{R_1 + R_2 + \frac{R_1 R_2}{R_L}} + \frac{V_1 R_2 - V_2 R_1}{R_L R_1 + R_L R_2 + R_1 R_2}\end{aligned} \tag{2}$$

Ideally, all DERs contribute power to the common load uniformly. The condition is held true when $V_1 = V_2$ and $R_1 = R_2$. However, in practice, the cable resistance cannot be the same, furthermore, the voltage mismatch can be caused by sensor errors [25]. Therefore, the current sharing difference among distributed converters shows up and results in the bus voltage deviation. The percentage of current-sharing error (eI) and voltage deviation (eV) are defined in (3) and (4) correspondingly [25]. These are considered as performance indices to compare the effectiveness of different droop strategies in the following sections.

$$eI = \mid \frac{I_1 - I_2}{I_1 + I_2} \mid \times 100\% = \mid \frac{\Delta I}{I_1 + I_2} \mid \times 100\% \tag{3}$$

$$eV = \frac{\mid V_{nom} - V_{bus} \mid}{V_{nom}} \times 100\% = \frac{\mid \Delta V \mid}{V_{nom}} \times 100\% \tag{4}$$

A. Linear droop control scheme

For load sharing purpose, the droop control inserts a virtual resistance at the converter output port, as shown in Fig. 3, where V_{nom} is the nominal DC bus voltage, $V_{out,n}$ and $I_{out,n}$ are the output voltage and current of the nth converter module, $C_v(s)$ represents the voltage regulator of converter, R_{Dn} and $G_{line,n}(s)$ are the equivalent droop resistance and line impedance of the nth converter module. It could be mathematically expressed as:

$$V_{ref,i} = V_{nom} - R_{Di} \times I_i \tag{5}$$

where V_i^{ref}, V^{nom}, R_{Di} and I_i represent the voltage reference, nominal bus voltage, virtual droop resistance and output current of the ith converter, respectively.

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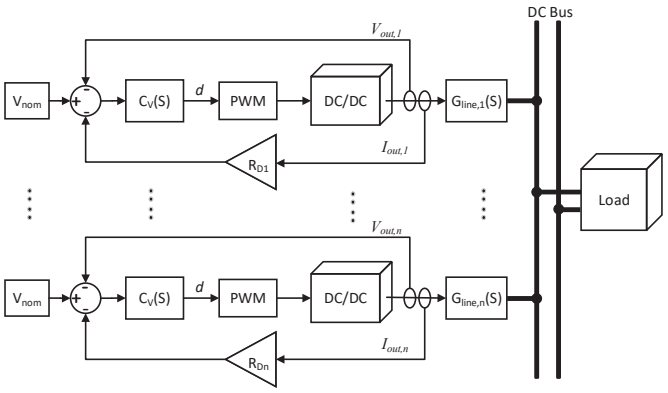

Fig. 3. Linear droop control and mimic of DC converters' control dynamics

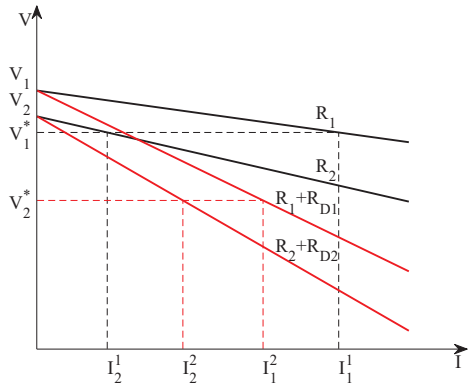

Fig. 4. Characteristics of linear droop controller

For the fixed voltage deviation (ΔV) and current rating (I_{max}), the virtual droop resistance can be determined by:

$$R_{Di} = \frac{\Delta V}{I_{max}} \tag{6}$$

Fig. 4 shows the linear droop characteristics curve, which depicts the relationship between the bus voltage and converter output current. When the droop control scheme is applied, the current sharing difference between two converters can be obtained from (2) by substituting $R_{total,1} = R_1 + R_{D1}$ and $R_{total,2} = R_2 + R_{D2}$:

$$\begin{aligned} \triangle I &= I_1 - I_2 \\ &= \frac{2(V_1 - V_2)}{R_{total,1} + R_{total,2} + \frac{R_{total,1}R_{total,2}}{R_L}} \\ &+ \frac{V_1 R_{total,2} - V_2 R_{total,1}}{R_L R_{total,1} + R_L R_{total,2} + R_{total,1}R_{total,2}} \end{aligned} \tag{7}$$

The high setting of the equivalent droop resistance (R_{D1} and R_{D2}) minimizes the current sharing difference $\triangle I$. However, the bus voltage deviation increases with the high droop gain. In summary, the constant droop gain is inflexible that cannot achieve high performance in terms of both precise load sharing and accurate voltage regulation, as discussed in [26].

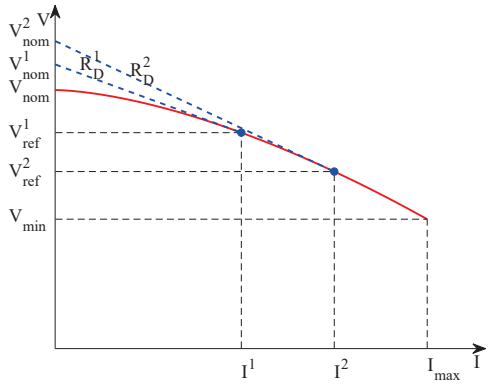

Fig. 5. Characteristics of nonlinear droop controller

B. Nonlinear droop control scheme

A nonlinear droop control scheme is proposed in [16] to improve the accuracy of voltage regulation. The droop characteristics curve is shown in Fig. 5, which tends to increase both equivalent droop gain and nominal voltage as the load current increases. The nonlinear droop equation is defined in (8), where I_i is the ith converter output current, m_i is the droop curve constant and a is the droop coefficient:

$$V_{ref,i} = V_{nom} - m_i I_i^a, \tag{8}$$

where $m_i = \dfrac{V_{nom} - V_{min}}{I_{max,i}^a}$.

The equivalent droop gain R_{Di} for different converter output current I_i can be expressed by taking the derivation of $V_{ref,i}$ with respect to I_i:

$$R_{Di} = \frac{\partial V_{ref,i}}{\partial I_i} = \frac{-a(V_{nom} - V_{min})}{I_{max,i}^a} I_i^{a-1} \tag{9}$$

The equivalent nominal voltage can be derived by calculating the intersection of voltage axis and equivalent linear droop line for the converter output current I_i:

$$V_{nom,i} = V_{nom} - m_i I_i^a + R_{Di} I_i \tag{10}$$

The droop coefficient a can be determined based on the maximum equivalent droop gain R_{max} when converter output current is maximum:

$$a = \frac{R_{max} I_{max,i}}{V_{nom} - V_{min}} \tag{11}$$

The determination of the maximum equivalent droop gain is related to the DC MG parameters (e.g. converter voltage deviation due to measurement and reference errors and cable resistances) and acceptable current sharing error. However, the equivalent droop gain is close to zero under light load condition, leading to a large current sharing error. The nonlinear droop controller with a larger R_{max} can achieve more accurate current sharing at a heavy load condition but less accurate current sharing accuracy at a light load condition compared to conventional linear droop control scheme. Hence, there is still a trade-off between the performance of the nonlinear droop approach at light load and heavy load conditions.

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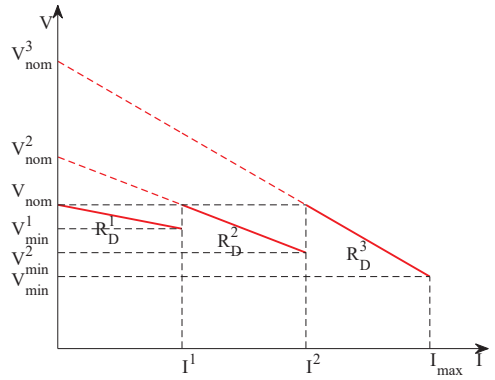

Fig. 6. Characteristics of proposed piecewise droop controller ($n = 3$)

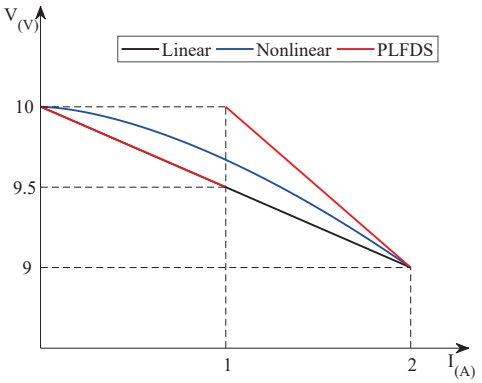

Fig. 7. Voltage reference comparison of droop schemes

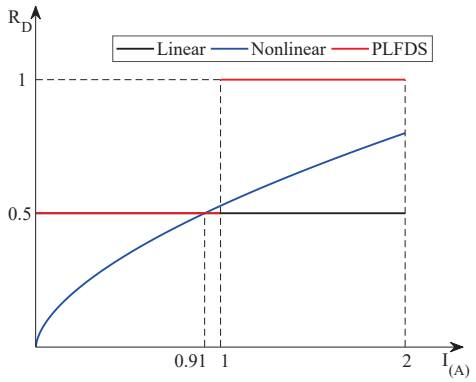

Fig. 8. Droop gain comparison of droop schemes

III. Piecewise Linear Formation

A piecewise linear formation of droop strategy (PLFDS) is proposed to achieve high and balanced performance for both voltage regulation and current sharing in DC MG. The performance indices defined in (3) and (4) are targeted to demonstrate the improvements. The PLFDS adopts the simple linear droop characteristics but divides into vertical segments uniformly, as shown in Fig. 6. In each segment, the equivalent nominal voltage and droop gain of the droop characteristics curve are updated locally and adaptively with the load conditions. The proposed droop equation for the voltage reference of individual converters is expressed by:

$$V_{ref,i} = V_{nom} - R^j_{Di}\Big(I_i - (j-1) \times I^j_{seg}\Big) \tag{12}$$

where V_{nom} is the nominal voltage, $V_{ref,i}$ and I_i are the ith converter output voltage reference and output current, and R^j_{Di} is the equivalent droop gain at the jth segment of the droop characteristics curve. The value of j increases discretely from 1 to n, where n is the number of segments. As the droop curve is divided uniformly, the width (I^j_{seg}) of all segments are identical, and the j can be derived by rounding up the result of converter output current divided by segment width:

$$I^j_{seg} = \frac{I_{max}}{n} \tag{13}$$

$$j = \left\lceil \frac{I_i}{I^j_{seg}} \right\rceil \tag{14}$$

It should be noted that in each segment, the voltage reference of proposed PLFDS controller should be higher than the corresponding voltage reference of conventional linear droop equation in (5) at the same current (I_i). For achieving better performance on voltage regulation, the minimum voltage reference (V^j_{min}) of PLFDS controller should be the same as the voltage reference of linear droop controller when the current is located at the jth barrier, and the local voltage deviation (ΔV^j) of each segment can be obtained based on the fixed global voltage deviation (ΔV) and maximum current (I_{max}):

$$V^j_{min} = V_{nom} - j \times I^j_{seg} \frac{\Delta V}{I_{max}} \tag{15}$$

$$\Delta V^j = V_{nom} - V^j_{min} \tag{16}$$

The local equivalent droop gain (R^j_D) can be determined by the local voltage deviation (ΔV^j) and the width (I^j_{seg}) of a single segment:

$$R^j_D = \frac{\Delta V^j}{I^j_{seg}} \tag{17}$$

The performance of PLFDS can be optimally tuned by varying the number of segments (n). When $n = 1$, it turns into a conventional linear droop controller and loses the flexibility for optimal tuning. As the value of n increases, the accuracy of current sharing and voltage regulation can be expected. For practical implementation, the value of n should be limited to avoid frequent transition among segments.

Fig. 7 and Fig. 8 depict the voltage reference and droop gain with a comparison of the aforementioned droop schemes in terms of standard linear and nonlinear approaches. The demonstration follows a simple case for easy understanding: a nominal voltage of $10V$, rate current of $2A$, a voltage deviation of $1V$, a maximum nonlinear droop gain of 0.8 and the PLFDS segments number of 2. The droop gain in the PLFDS scheme can be tuned separately for the balanced performance of voltage regulation and load sharing.

Fig. 7 shows that the PLFDS provides the highest droop gain and the lowest voltage deviation compared to the linear and nonlinear droop schemes when the current is in range from

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1 A to 2 A. Furthermore, The droop gain of the PLFDS can be tuned the same as the standard linear solution for the range from 0 to 1 A. It shows that the voltage deviation of PLFDS is maintained the same as that of linear droop scheme when the current is no more than 1 A.

It is also evident from Fig. 8 that when the current is less than $0.91A$, the PLFDS and linear droop scheme has the same droop gain, which is higher than nonlinear droop scheme's droop gain. It shows that the load sharing performance is better than the nonlinear droop solution. When the current is between $0.91A$ and $1A$, the nonlinear droop scheme offers higher droop gain than the PLFDS and linear droop schemes. When the current is higher than $1A$, the PLFDS provides higher droop gain than the linear and nonlinear droop schemes.

In summary, the PLFDS offers a balanced improvement in term of low voltage deviation and accurate current sharing accuracy than linear and nonlinear droop schemes when the load current is high. When the load current is low, the PLFDS is adjustable for better current sharing accuracy and adjustable voltage deviation to balance the performance indices, as defined in (3) and (4). The case study is simple and based on 2-segment PLFDS. With the increasing number of segments, the PLFDS shows the capability and potential to be tuned to match the same deviation as the nonlinear droop method.

A. Hysteresis loop for robust transition

In practical systems, sensing error, disturbance and noise can lead to fault transition when the converter output current is close to the barriers between segments. In order to prevent any fault transition between segments, a hysteresis loop is implemented and shown as:

$$j = \begin{cases} j_{pre} - 1 & I_i - j_{pre} \times I_{seg}^{j_{pre}} < e_- \\ j_{pre} & e_- < I_i - j_{pre} \times I_{seg}^{j_{pre}} < e_+ \\ j_{pre} + 1 & I_i - j_{pre} \times I_{seg}^{j_{pre}} > e_+ \end{cases} \quad (18)$$

where j is the input to the decision in (12), j_{pre} is the previous segment number, I_{seg} is the segment width, e_- and e_+ are the hysteresis loop errors. If the difference between present current (I_i) and the multiply of previous segment number (j_{pre}) and segment width (I_{seg}) is higher than the positive hysteresis loop error (e_+), the present segment number (j) can be increased by one; if the difference is lower than the negative hysteresis loop error (e_-), the present segment number (j) can be increased by one; otherwise, the segment number (j) remains the same.

B. Slew-rate limiter

Sudden change of load can lead to significant transient behaviour of the PLFDS due to the shift between segments and the sudden change of the voltage reference. The slew-rate limiter should be defined and tuned to regulate the transient and eliminate any windup effect caused by a sudden change of the reference value. The response time to the setpoint change can be predicted by analysing the closed-loop dynamics. Then, the slew rate limiter can be designed with two degrees of freedom based on the predicted response speed.

TABLE I
PARAMETERS FOR STABILITY ANALYSIS

Parameters	Symbol	Value
Nominal voltage	V_{nom}	10 V
Load current	I_L	4 A
Load resistance	R_L	2.5 Ω
Bus voltage deviation	ΔV	1 V
Rate current	I_{max}	2 A
Number of segments	n	2
Line resistance 1	R_1	0.1 Ω
Line resistance 2	R_2	0.1 Ω
Line inductance 1	L_1	0.2 mH
Line inductance 2	L_2	0.2 mH

IV. DYNAMIC ANALYSIS

In this section, the system dynamics is investigated in all operating conditions by small-signal analysis to guarantee the reliable performance of DC MG. The load of DC MG behaves as a constant power load (CPL) when the converters regulate their output in the steady state according to the study in [27], [28]. However, the negative incremental resistance of CPL can cause negative impedance instability for DC MG, which has been reported in [29], [30].

A system based on two converters supplying a load is utilized for the demonstration of dynamic analysis, shown in Fig. 3. The control dynamic structure of PLFDS is similar to that of linear droop scheme except for the adaptive virtual droop resistances. The system parameters are shown in Table I. Eigenvalue approach is employed to reveal the critical dynamic in the DC MG. Applying the small signal modelling to (12) yields:

$$\tilde{v}_{ref,i} = -R_{Di}^{j} \tilde{i}_i \quad (19)$$

The state-space model can be constructed and shown as the state matrix:

$$A = \begin{bmatrix} \frac{-R_{D1}^{j}\tilde{i}_1 - R_L - R_1}{L_1} & -\frac{R_L}{L_1} \\ -\frac{R_L}{L_2} & \frac{-R_{D2}^{j}\tilde{i}_2 - R_L - R_2}{L_2} \end{bmatrix} \quad (20)$$

Fig. 9 depicts the locus of dominant eigenvalues when the equivalent load resistance changes. The changes of pole locations caused by the variation of load resistance can be neglected for both segments of the PLFDS. Fig. 10a and Fig. 10b show the locus of dominant eigenvalues when the cable resistances and inductances vary from 50% to 200% of the values shown in Table I. The dominant eigenvalues move away from the imaginary axis when the cable resistances increase, while they move away towards the imaginary axis when the cable inductances increase. With the same parameters, eigenvalues of the $2nd$ segment show better stability margin. Generally, it can be seen that the real part of the dominant eigenvalues is negative, proving the stability of the system under the variation of load and cable parameters.

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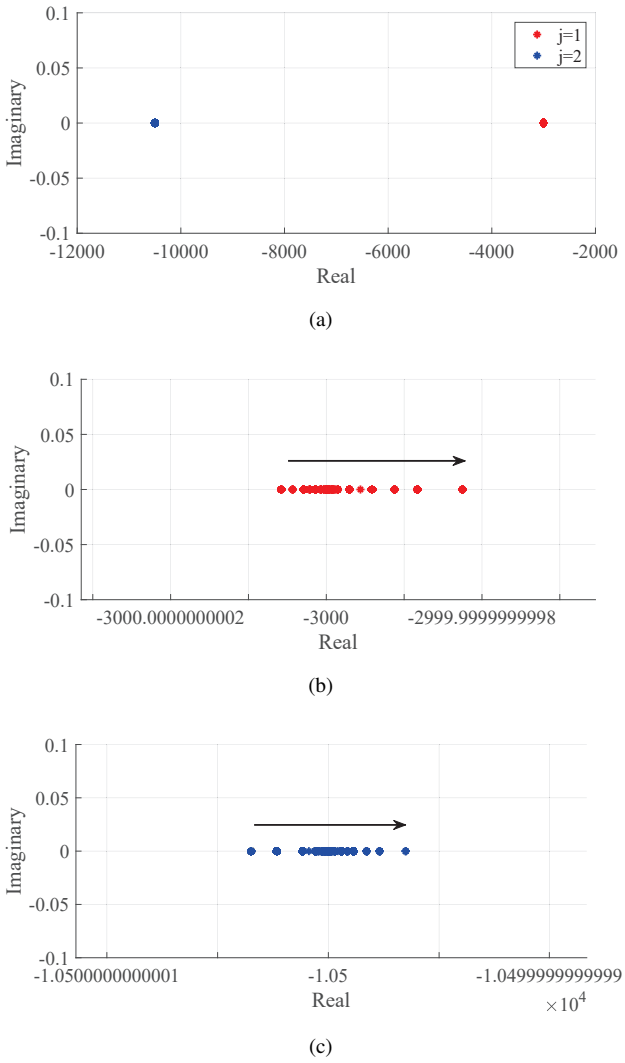

Fig. 9. Locus of dominant eigenvalue for the control system increasing load R_L (a) both the $1st$ segment ($j = 1$) and the $2nd$ segment ($j = 2$), (b) the $1st$ segment ($j = 1$), (c) the $2nd$ segment ($j = 2$)

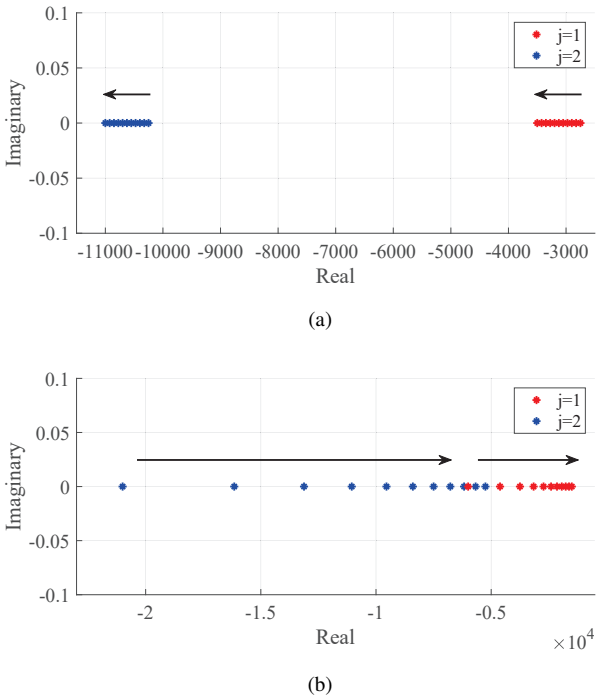

Fig. 10. Locus of dominant eigenvalue for the control system (a) increasing cable resistance R_1 and R_2, (b) increasing cable inductance L_1 and L_2

TABLE II
DC MG SIMULATION PARAMETERS

Parameters	Symbol	Value
Nominal voltage	V_{nom}	380 V
Bus voltage deviation	ΔV	5 V
Rate current	I_{max}	10 A
Switching frequency	f_{sw}	100 kHz
Converter inductance	L	3 mH
Converter capacitor	C	3.3 μF
Bus capacitor	C_{bus}	1.8 mF
Line resistance 1	R_1	0.1 Ω
Line resistance 2	R_2	0.3 Ω

V. EVALUATIONS

To verify the performance of proposed PLFDS, evaluation includes both simulation for a 7.6kW DC MG and experimental test based on a scale-down lab setup.

A. Simulation Evaluations

The $7.6kW$ DC MG is shown in Fig. 1 with the parameters shown in Table II. The simulation is based on the platform of MATLAB/Simulink. The linear droop gain is selected as 0.5 based on (6), the maximum nonlinear droop gain is selected as 0.8 in order to have acceptable load sharing accuracy and stability at light load conditions and the section numbers of PLFDS is selected as 2 for evaluation. The PLFDS implementation follows the scheme, as shown in Fig. 6 and the schematics of two parallel converter system, as shown in Fig. 3.

Fig. 11 shows the simulation results of the DC MG during load switching between light load condition ($2A$) and heavy load condition ($18A$). During step changes, the proposed PLFDS demonstrates stable transition without any overshoot. The settling times for PLFDS also remains of the same order: the settling time for PLFDS when taking a step change from $18A$ to $2A$ and from $2A$ to $18A$ are $1.9ms$ and $5.1ms$ respectively, while those of linear droop scheme are $3ms$ and $4.1ms$ and nonlinear droop scheme's settling times are $1.9ms$ and $5.2ms$ correspondingly.

Fig. 12 and 13 present the comparison of DC bus voltage deviation (eV) and current sharing error (eI) defined in (3) and (4) at different load conditions. It can be seen that the proposed FLFDS demonstrates good current sharing and considerable voltage regulation under all loading conditions. When the magnitude of load current is lower than $10A$, which is the light load, the performance of linear droop scheme and PLFDS is almost the same, and nonlinear droop scheme shows better voltage regulation but poorer current sharing accuracy. When the magnitude of load current is higher than $10A$, which is the

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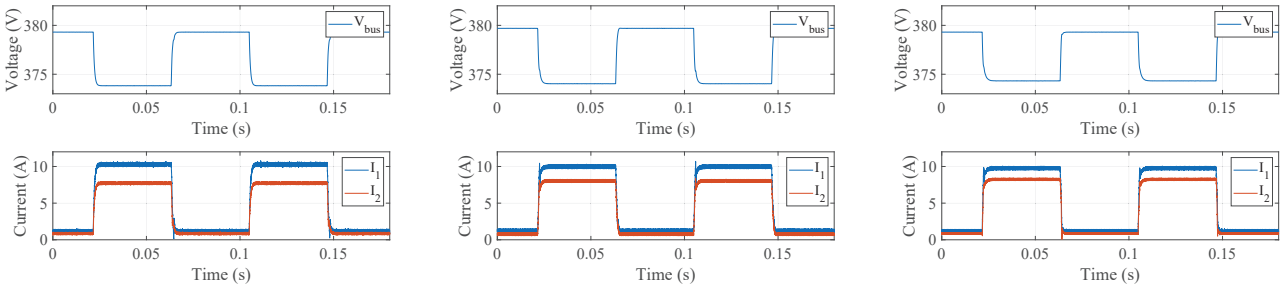

Fig. 11. Simulation results: converter output current (5 A/div) and DC-bus voltage (2 V/div) during step changes in load between 2A to 18A (a) Linear, (b) Nonlinear, (c) PLFDS

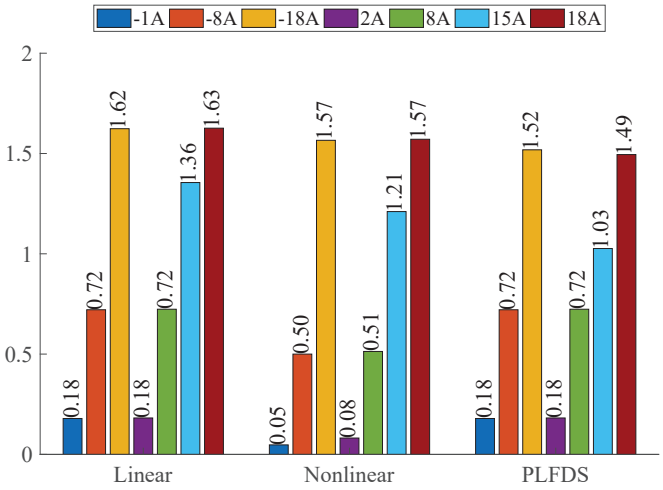

Fig. 12. Simulation results: voltage deviation comparison of the droop schemes (%)

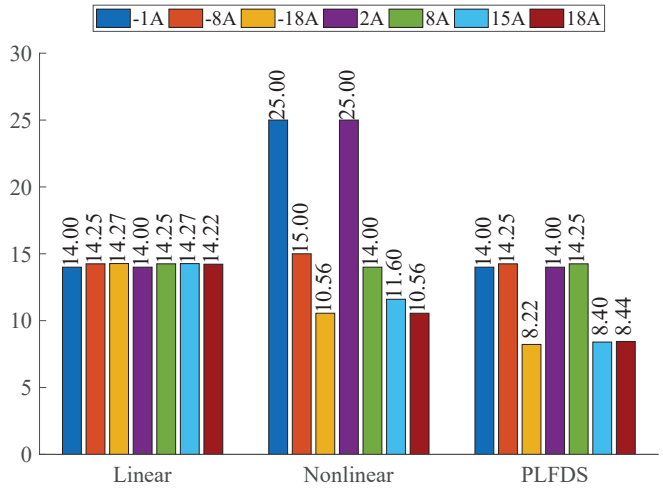

Fig. 13. Simulation results: current sharing accuracy comparison of the droop schemes (%)

heavy load, the proposed PLFDS produces the best balance between the current sharing and voltage regulation among all methods.

B. Experimental Evaluations

A scaled-down experimental prototype is constructed with two synchronous buck converters to demonstrate the operation of PLFDS and evaluate its performance. The experimental setup is shown in Fig. 14. The prototype parameters are listed in Table III, and the droop parameters are exactly the same as those of simulation tests. The Hall effect sensor is used for the current measurement, which is the IC model $ACS724xLLCTR-10AU$ with the sensitivity error of 1%. The voltage measurement is formed by the resistor divider with 1% tolerance. Both current and voltage sensors are implemented with a signal conditioner for the high accuracy and robust signal transmission.

The control algorithm is implemented in a digital signal processing (DSP) board TMS320F28335, and two control loops

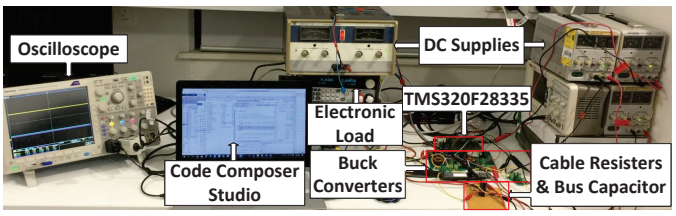

Fig. 14. Scaled-down experimental prototype of a DC MG with two DC-DC buck converters in parallel

are independently executed for both converters to regulate their output voltage. Fig. 15 shows the dynamic transient during a step change of load from the current of 3A to 1A. During the step change, the proposed control scheme remains superior performance as the conventional droop methods. No overshoot is sensed and the $6ms$ settling time remains the same as the two conventional droop controllers.

Fig. 16 and 17 show DC bus voltage deviation and current sharing accuracy performance comparison at light and heavy

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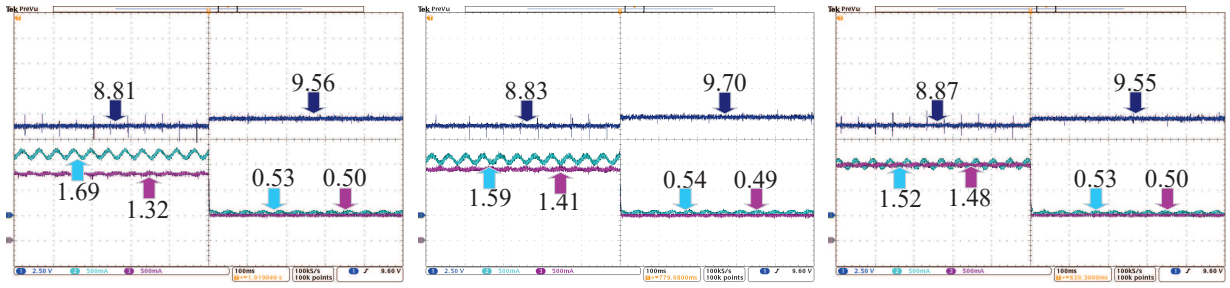

(a) (b) (c)

Fig. 15. Experimental results: converter output current (500 mA/div) and DC-bus voltage (2.5 V/div) during a step change in load from 3A to 1A (a) Linear, (b) Nonlinear, (c) PLFDS

TABLE III
DC MG EXPERIMENTAL PARAMETERS

Parameters	Symbol	Value
Nominal voltage	V_{nom}	10 V
Bus voltage deviation	ΔV	1 V
Rate current	I_{max}	2 A
Switching frequency	f_{sw}	75 kHz
Converter inductance	L	1.3 mH
Converter capacitor	C	3.3 μF
Bus capacitor	C_{bus}	1.8 mF
Line resistance 1	R_1	0.2 Ω
Line resistance 2	R_2	0.33 Ω

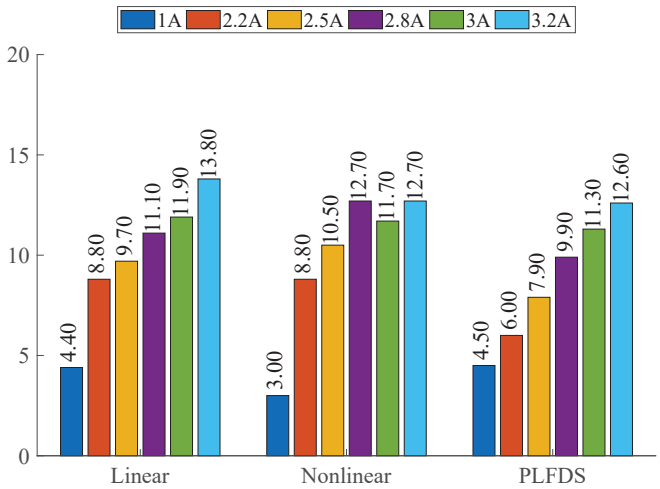

Fig. 16. Experimental results: voltage deviation comparison of the droop schemes (%)

load conditions. When the load current is less than $2A$, which is the light load, the difference between the performance of PWD and linear droop controllers can be neglected because the first segment of the PLFDS characteristic curve is the same as that of the linear droop controller. Comparing to the counterpart of the nonlinear droop controller, the PLFDS achieves significant improvement on the load sharing accuracy but maintains the voltage regulation the same as the conventional linear droop approach.

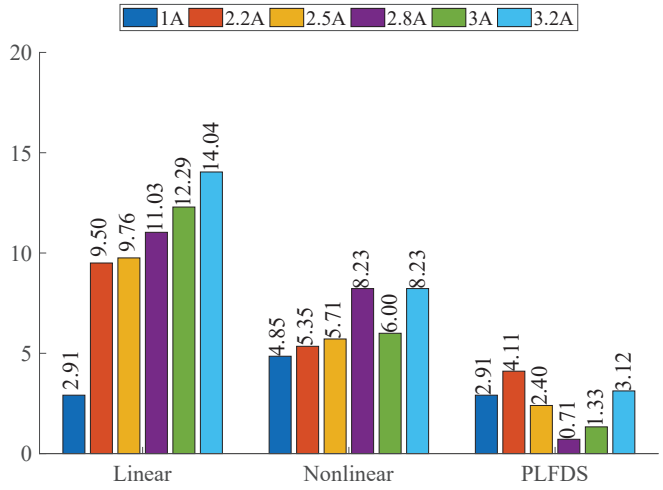

Fig. 17. Experimental results: current sharing accuracy comparison of the droop schemes (%)

When the load current is higher than $2A$, which is the heavy load, the experimental evaluation shows that both the current-sharing error and voltage deviation are the minimum for the proposed strategy.

Conclusively, it can be observed that the proposed PLFDS can achieve better current sharing and voltage deviation at heavy load condition and overcome the weakness of nonlinear droop control scheme at light load condition.

VI. CONCLUSION

In this paper, a new droop control strategy is presented for DC MG, which is constructed by the piecewise linear formation. The proposed solution demonstrates the flexibility for an improved balance in terms of both current sharing accuracy and DC voltage steadiness. The hysteresis loop and slew-rate limited are included in the proposed scheme to improve system robustness. The system analysis and design are given in details, where the small-signal analysis is adopted to reveal system dynamics for stable and robust control loop

design. Simulation and experimental results support the effectiveness of the proposed control scheme in comparison with the existing solutions in terms of the linear droop controller and nonlinear droop method. The proposed scheme focuses on droop technology but can be combined with other technologies to achieve improved overall coordination performance.

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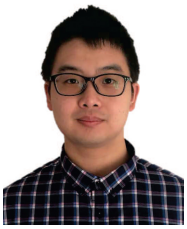

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